



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
[www.uspto.gov](http://www.uspto.gov)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/603,375	06/25/2003	Jong Goo Jung	30205/39379	2815
4743	7590	03/16/2005	EXAMINER	
MARSHALL, GERSTEIN & BORUN LLP 6300 SEARS TOWER 233 S. WACKER DRIVE CHICAGO, IL 60606				DOTY, HEATHER ANNE
			ART UNIT	PAPER NUMBER
			2813	

DATE MAILED: 03/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding..

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/603,375	JUNG, JONG GOO	

  

<b>Examiner</b>	<b>Art Unit</b>	
Heather A. Doty	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1) Responsive to communication(s) filed on 10 November 2004.  
 2a) This action is FINAL.                    2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4) Claim(s) 1-8 and 10-19 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) Claim(s) \_\_\_\_\_ is/are allowed.  
 6) Claim(s) 1-8 and 10-19 is/are rejected.  
 7) Claim(s) \_\_\_\_\_ is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on 25 June 2003 is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____
3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date <u>6/25/03</u> .	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
	6) <input type="checkbox"/> Other: _____

**DETAILED ACTION**

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-3, 5, 6-8, 11, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art (APA) in view of Nojo et al. (U.S. 6,443,811).

With respect to claim 1, APA teaches a method for manufacturing a metal line contact plug of a semiconductor device, the method comprising: depositing a conductive material for a wordline on a semiconductor structure (page 2, lines 1-2); forming a wordline pattern by depositing a hard mask nitride film on an overlapping portion of the conductive material for the wordline (page 2, lines 2-3); forming a nitride spacer on a sidewall of the wordline pattern (page 2, line 6; 5 in Fig. 1B); forming a planarized interlayer insulating film on the upper portion of the wordline pattern (page 2, lines 6-10); forming a contact hole by etching the interlayer insulating film when the substrate is exposed (page 2, lines 11-12; 8 in Fig. 1C); forming a silicon layer on the surface of the interlayer insulating film where the contact hole is formed (page 2, lines 19-20; 9 in Fig. 1E); performing a primary CMP process on the silicon layer using a first slurry for an oxide film until the interlayer insulating film is exposed (page 2, lines 23-27); and performing a secondary CMP process on the silicon layer and the interlayer insulating

Art Unit: 2813

film using a common slurry for an oxide film until the hard mask film is exposed (page 2, lines 28-30).

APA does not teach that the second CMP slurry includes a solvent, an abrasive dispersed in the solvent, and an alkyl ammonium salt ( $R_{(4-n)}H_nN^+X^-$ , wherein n is an integer ranging from 0 to 3).

Nojo et al. teaches a CMP slurry to polish oxides including a solvent (water, column 2, line 21), an abrasive dispersed in the solvent (ceria, column 2, line 21), and an alkyl ammonium salt (for example, hexadecyl-trimethyl ammonium chloride, column 4, Table 1).

Therefore, at the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the method for manufacturing a metal line contact plug of a semiconductor device as taught by APA with the oxide-polishing slurry composition taught by Nojo et al. The motivation for doing so at the time of the invention would be to improve defect control on semiconductor wafers, as expressly taught by Nojo et al. (column 1, lines 14-15).

With respect to claims 2 and 3, APA and Nojo et al. together teach the method according to claim 1 (note 35 U.S.C. 103(a) rejection above). Nojo et al. further teaches that R of the alkyl ammonium salt is selected from the group consisting of C<sub>6</sub>-C<sub>18</sub> (column 3, line 43), which falls in the ranges C<sub>1</sub>-C<sub>50</sub> (claim 2) and C<sub>1</sub>-C<sub>20</sub> (claim 3).

With respect to claim 5, APA and Nojo et al. together teach the method according to claim 1 (note 35 U.S.C. 103(a) rejection above). Nojo et al. further teaches that the X<sup>-</sup> of the alkyl ammonium salt is Cl<sup>-</sup> or Br<sup>-</sup> (column 4, Table 1). At the time of the invention,

it would have been obvious to one of ordinary skill in the art to combine the teachings of APA and Nojo et al. to obtain the invention as specified in claim 5 for the reasons given above.

With respect to claim 6, APA and Nojo et al. together teach the method according to claim 1 (note 35 U.S.C. 103(a) rejection above). Nojo et al. further teaches that the alkyl ammonium salt is hexadecyl-trimethyl ammonium chloride (column 4, Table 1), which is the same as cetyltrimethylammonium chloride. At the time of the invention, it would have been obvious to one of ordinary skill in the art to combine the teachings of APA and Nojo et al. to obtain the invention as specified in claim 6 for the reasons given above.

With respect to claim 7, APA and Nojo et al. together teach the method according to claim 1 (note 35 U.S.C. 103(a) rejection above). Nojo et al. further teaches that the alkyl ammonium salt (cationic surfactant) is present in an amount 0.01 wt% based on the CMP slurry (column 5, lines 29-31), which is included in the range 0.01 to 10 wt%. At the time of the invention, it would have been obvious to one of ordinary skill in the art to combine the teachings of APA and Nojo et al. to obtain the invention as specified in claim 7 for the reasons given above.

With respect to claim 8, APA and Nojo et al. together teach the method according to claim 7 (note 35 U.S.C. 103(a) rejection above). Nojo et al. further teaches that the alkyl ammonium salt (cationic surfactant) is present in an amount 0.01 wt% based on the CMP slurry (column 5, lines 29-31), which is included in the range 0.01 to 1 wt%. At the time of the invention, it would have been obvious to one of ordinary skill in the art to

combine the teachings of APA and Nojo et al. to obtain the invention as specified in claim 8 for the reasons given above.

With respect to claim 11, APA and Nojo et al. together teach the method according to claim 1 (note 35 U.S.C. 103(a) rejection above). Nojo et al. further teaches a neutral slurry (column 2, line 22), which by definition has a pH of 7, and is thus included in the pH range 2 to 7. At the time of the invention, it would have been obvious to one of ordinary skill in the art to combine the teachings of APA and Nojo et al. to obtain the invention as specified in claim 11 for the reasons given above.

With respect to claim 12, APA and Nojo et al. together teach the method according to claim 1 (note 35 U.S.C. 103(a) rejection above). Nojo et al. further teaches that the slurry is in the alkaline range (column 3, line 37), which is included in the pH range 8 to 12. At the time of the invention, it would have been obvious to one of ordinary skill in the art to combine the teachings of APA and Nojo et al. to obtain the invention as specified in claim 12 for the reasons given above.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's prior art (APA) in view of Vogt et al. (U.S. 2002/0170237).

As noted above, APA teaches a method for manufacturing a metal line contact plug of a semiconductor device, the method comprising: depositing a conductive material for a wordline on a semiconductor structure (page 2, lines 1-2); forming a wordline pattern by depositing a hard mask nitride film on an overlapping portion of the conductive material for the wordline (page 2, lines 2-3); forming a nitride spacer on a sidewall of the wordline pattern (page 2, line 6; 5 in Fig. 1B); forming a planarized

interlayer insulating film on the upper portion of the wordline pattern (page 2, lines 6-10); forming a contact hole by etching the interlayer insulating film when the substrate is exposed (page 2, lines 11-12; 8 in Fig. 1C); forming a silicon layer on the surface of the interlayer insulating film where the contact hole is formed (page 2, lines 19-20; 9 in Fig. 1E); performing a primary CMP process on the silicon layer using a first slurry for an oxide film until the interlayer insulating film is exposed (page 2, lines 23-27); and performing a secondary CMP process on the silicon layer and the interlayer insulating film using a common slurry for an oxide film until the hard mask film is exposed (page 2, lines 28-30).

APA does not teach that the second CMP slurry includes a solvent, an abrasive dispersed in the solvent, and an alkyl ammonium salt ( $R_{(4-n)}H_nN^+X^-$ , wherein n is an integer ranging from 0 to 3). APA also does not teach that the R includes an unsaturated alkyl group having at least one or more of a double bond or triple bond.

Vogt et al. teaches a CMP slurry for polishing silica films (paragraph 9) including a solvent (deionized water, paragraph 19), an abrasive (silica, paragraph 8), and an ammonium salt  $R_4N^+X^-$ , where R is alkyl (paragraph 8), making the salt an alkyl ammonium salt, as in claim 1. R can also be alkenyl (paragraph 8), an unsaturated alkyl group having a double bond, as in claim 4.

Therefore, at the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the method for manufacturing a metal contact plug of a semiconductor device as taught by APA with the CMP slurry composition taught by Vogt et al. to obtain the invention as taught by claim 4. The motivation for doing so at

the time of the invention would have been to provide a polishing slurry for chemical-mechanical polishing with a high polishing rate and a low surface roughness of the substrate, as expressly taught by Vogt et al. (paragraph 6).

Claims 10 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art (APA) in view of Misra et al. (US 6,471,735).

With respect to claim 10 and as noted above, APA teaches a method for manufacturing a metal line contact plug of a semiconductor device, the method comprising: depositing a conductive material for a wordline on a semiconductor structure (page 2, lines 1-2); forming a wordline pattern by depositing a hard mask nitride film on an overlapping portion of the conductive material for the wordline (page 2, lines 2-3); forming a nitride spacer on a sidewall of the wordline pattern (page 2, line 6; 5 in Fig. 1B); forming a planarized interlayer insulating film on the upper portion of the wordline pattern (page 2, lines 6-10); forming a contact hole by etching the interlayer insulating film when the substrate is exposed (page 2, lines 11-12; 8 in Fig. 1C); forming a silicon layer on the surface of the interlayer insulating film where the contact hole is formed (page 2, lines 19-20; 9 in Fig. 1E); performing a primary CMP process on the silicon layer using a first slurry for an oxide film until the interlayer insulating film is exposed (page 2, lines 23-27); and performing a secondary CMP process on the silicon layer and the interlayer insulating film using a common slurry for an oxide film until the hard mask film is exposed (page 2, lines 28-30).

APA does not teach that the second CMP slurry includes a solvent, an abrasive dispersed in the solvent, and an alkyl ammonium salt ( $R_{(4-n)}H_nN^+X^-$ , wherein n is an integer ranging from 0 to 3). APA also does not teach that the abrasive is  $Al_2O_3$ .

Misra et al. teaches a CMP slurry to polish oxides including a solvent (water, column 7, line 35), an abrasive dispersed in the solvent (column 8, line 1), and an alkyl ammonium salt (alkyl ammonium hydroxide) (column 3, line 15). Misra et al. expressly teaches that the abrasive is  $Al_2O_3$  (aluminum oxide, column 8, line 1).

Therefore, at the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the method for manufacturing a metal line contact plug of a semiconductor device taught by APA with the oxide-polishing slurry composition, wherein the abrasive is  $Al_2O_3$ , taught by Misra et al., to obtain the invention as specified in claim 10 (including claim 1). The motivation for doing so at the time of the invention would have been to increase the oxide-to-silicon nitride polish rate selectivity during the polishing of a semiconductor substrate (column 3, lines 23-28), as expressly taught by Misra et al.

With respect to claim 19, APA and Misra et al. together teach the method according to claim 1 (note 35 U.S.C. 103(a) rejection above). Misra et al. further teaches that the CMP process is performed using a hard pad (column 3, line 34). At the time of the invention, it would have been obvious to one of ordinary skill in the art to combine the teachings of APA and Misra et al. to obtain the invention as specified in claim 19 for the reasons given above.

Art Unit: 2813

Claims 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's applied prior art (APA) in view of Nojo et al. (U.S. 6,443,811) as applied to claim 1 above, and further in view of Cho et al. (U.S. 6,784,062).

With respect to claim 13, APA and Nojo et al. together teach the method according to claim 1 (note 35 U.S.C. 103(b) rejection above), but do not teach that the conductive material is selected from the group consisting of doped silicon, poly-silicon, tungsten (W), tungsten nitride (WN), tungsten silicide ( $WSi_x$ ), and titanium silicide ( $TiSi_x$ ).

Cho et al. teaches a method for fabricating transistors including forming a wordline, wherein the conductive material is tungsten silicide ( $WSi_x$ ) (column 3, lines 8-9; **24** in Fig. 3).

Therefore, at the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the method for manufacturing a metal line contact plug of a semiconductor device as in claim 1 and as taught by APA and Nojo et al. with the method of forming a wordline wherein the conductive material is tungsten silicide, as taught by Cho et al. The motivation for doing so at the time of the invention would have been to fabricate a device with desirable transistor gate profiles, as expressly taught by Cho et al. (column 1, lines 42-43).

With respect to claim 14, APA and Nojo et al. together teach the method according to claim 1 (note 35 U.S.C. 103(b) rejection above), but do not teach that the wordline pattern is formed by an etching process using  $CCl_4$  or  $Cl_2$  gas.

Cho et al. teach a method for fabricating transistors including forming a wordline, wherein the wordline pattern is formed by an etching process using Cl<sub>2</sub> gas, which has a high selectivity to a gate oxide (column 3, lines 27-34).

Therefore, at the time of the invention it would have been obvious to a person of ordinary skill in the art to combine the method for manufacturing a metal line contact plug of a semiconductor device as in claim 1 and as taught by APA and Nojo et al. with the method of forming a wordline, wherein the wordline pattern is formed by an etching process using Cl<sub>2</sub> gas, as taught by Cho et al., to obtain the invention as specified in claim 14. The motivation for doing so at the time of the invention would have been to use an etch with a high selectivity to an oxide, as noted above as expressly taught by Cho et al.

Claims 15, 16, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's applied prior art (APA) in view of Nojo et al. (U.S. 6,443,811) as applied to claim 1 above, and further in view of Wolf (*Silicon Processing for the VLSI Era*, v. 1-2, 1986, 1990).

With respect to claim 15, APA and Nojo et al. together teach the method according to claim 1 (note 35 U.S.C. 103(b) rejection above), but do not teach that the spacer is formed of TEOS or silane-based oxide films.

Wolf teaches forming spacers by silicon nitride deposition by PECVD using silane (SiH<sub>4</sub>) (v. 2, page 212, which incorporates by reference v. 1, chapter 6; v. 1, page 193, last paragraph – page 194, first paragraph).

Therefore, at the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the method for manufacturing a metal line contact plug of a semiconductor device as in claim 1 and as taught by APA and Nojo et al. with the method of forming a spacer of a silane-based oxide film, as taught by Wolf. The motivation for doing so at the time of the invention would have been to achieve good step coverage, as expressly taught by Wolf (v. 2, page 212, first paragraph).

With respect to claim 16, APA and Nojo et al. together teach the method according to claim 1 (note 35 U.S.C. 103(b) rejection above), but do not teach that the interlayer insulating film is selected from the group consisting of BPSG, PSG, PE-TEOS, PE-SiH<sub>4</sub>, HDP USG, HDP PSG, and APL oxide.

Wolf teaches that interlayer metals are commonly formed of BPSG to achieve a nearly planar surface (v. 2, page 196, first and second paragraphs), PSG to reduce stress in the oxide film (v. 2, pg. 197, first full paragraph), or PE-TEOS to alleviate cusping (v.2, page 198, second full paragraph).

Therefore, at the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the method for manufacturing a metal line contact plug of a semiconductor device as in claim 1 and as taught by APA and Nojo et al. with Wolf's cited materials for forming interlayer dielectrics. The motivation for doing so at the time of the invention would have been to achieve an almost planar surface, to reduce stress in the oxide film, or to alleviate cusping, as noted above and expressly taught by Wolf.

With respect to claim 18, APA and Nojo et al. together teach the method according to claim 1 (note 35 U.S.C. 103(b) rejection above), but do not teach that the silicon layer is formed of doped silicon or poly-silicon using a SiH<sub>4</sub> or Si<sub>2</sub>H<sub>6</sub> source.

Wolf teaches a method of forming doped silicon (v. 1, page 136-137) layers using a SiH<sub>4</sub> source (v. 1, page 143, last full paragraph).

Therefore, at the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the method for manufacturing a metal line contact plug of a semiconductor device as in claim 1 and as taught by APA and Nojo et al. with the method of forming doped silicon layers using a SiH<sub>4</sub> source, as taught by Wolf. The motivation for doing so at the time of the invention would have been to deposit silicon layers without undesirable pattern shifting, as taught by Wolf (v.1, page 143, last full paragraph).

Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art (APA) in view of Nojo et al. (U.S. 6,443,811) as applied to claim 1 above, and further in view of Cui et al. (U.S. 5,965,463).

With respect to claim 17, APA and Nojo et al. together teach the method according to claim 1 (note 35 U.S.C. 103(a) rejection above). They do not teach that the contact hole is formed by an etching process using a C<sub>4</sub>F<sub>8</sub>, C<sub>2</sub>F<sub>6</sub>, or C<sub>3</sub>F<sub>8</sub> source.

Cui et al. teaches a method of selectively etching silicon oxide over silicon to form contact holes using C<sub>4</sub>F<sub>8</sub> or C<sub>2</sub>F<sub>6</sub> (column 2, lines 6-7, 19-22).

Therefore, at the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the method for manufacturing a metal line contact plug

of a semiconductor device as in claim 1 and as taught by APA and Nojo et al. by using C<sub>4</sub>F<sub>8</sub> or C<sub>2</sub>F<sub>6</sub> to etch contact holes, as taught by Cui et al., to obtain the invention as specified in claim 17. The motivation for doing so at the time of the invention would have been to use an etch chemistry that will selectively etch silicon oxide over silicon, as expressly taught by Cui et al.

***Response to Arguments***

Applicant's arguments with respect to claims 1-19 have been considered but are moot in view of the new ground(s) of rejection.

### **Conclusion**

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. *Hackh's Chemical Dictionary*, edited by Julius Grant, provides a definition for "cetyl" that includes "Hexadecyl".

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Heather A. Doty, whose telephone number is 571-272-8429. The examiner can normally be reached on M-F, 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

had

  
ERIK KIELIN  
PRIMARY EXAMINER